



GDS Layer Convention for MPW Submission

NQCP superconducting-circuit fab (SC fab) — required layer numbering for every submitted design

Current revision: 2026-06-04 · Fully compatible with SC fab protocol v0.1.1, with room reserved for in-situ steps
· Source: NQCP internal wiki, "GDS Layer Convention"

Every design submitted to this multi-project wafer (MPW) run must use the layer numbers below. This is a fixed convention set by the fab process, not a per-design choice — a submission that draws its own geometry on the correct layer *numbers* can be fabricated on the shared process regardless of what your own design tool happens to call those layers internally.

Scope of this document: layers 70 and above (indium bumps, interposer fab steps, in-situ stencils) are not part of this MPW submission scheme and are omitted below. The full convention, including those ranges, is in the source wiki page.

General Convention

The layer number ranges below group related fabrication steps. Not every number in a range is necessarily in use — see the detailed table for exactly which ones are defined.

Layer Number	Description
01–09	Chip Outlines (passive layer)
10–19	Alignment Markers
20–29	Ground plane etch
30–39	JJ Layers (horizontal, vertical)
40–49	Patch layers
50–59	Airbridge feet layers
60–69	Airbridge etchback layers

If you're unsure which layer to use: if you're unsure which specific layer within a range applies to your design, place the element on the layer within that range closest to what you can recognize it as, rather than leaving it off the design entirely. Getting the correct ten's-range matters most for fabrication — every layer in a given range goes through the same physical process together (e.g. everything in 20–29 goes through ground-plane etch together, everything in 30–39 goes through the JJ process together), so a reasonable choice within the right range is workable even if the exact number isn't a perfect match. When in doubt, ask the MPW organizer rather than guess at a different range entirely.

Standard Layer Convention for SC Fab

A .lyp layer convention file is a KLayout configuration file that defines how each layout layer is named, colored, and displayed. The table below is the content of the canonical file for this revision.

SC_layer_04jun2026.lyp

Layer	Shorthand name	Description
00	outline_Q	Q-Chip Boundary, the bounding box which defines final chip dimensions (after eventual dicing).
01	outline_MCM	MCM-Chip Boundary, the bounding box which defines final chip dimensions (after eventual dicing).
02	outline_Interposer	Interposer-Chip Boundary, the bounding box which defines final chip dimensions (after eventual dicing).
10	inner_marks	Inner alignment marks, exposed with a lower e-beam current for higher resolution.
11	outer_marks	Outer alignment marks, dice marks and global wafer-level marks.
20	GP_consolidation	Consolidation layer for the MCM-plane. Defines the areas of the ground plane which will be exposed and etched (subtractive).
21	GP_Q_metal	Additive layer for the Q-plane. The areas of the Q-plane where metal will remain.
22	GP_MCM_metal	Additive layer for the MCM. The areas of the MCM where metal will remain.
23	GP_Q_etch	Subtractive layer for the Q-plane. Defines the areas of the ground plane which will be etched.
24	GP_MCM_etch	Subtractive layer for the MCM-plane. Defines the areas of the ground plane which will be etched.
26	fluxholes_Q	Subtractive layer for the Q-plane. This layer should only contain flux holes.
27	fluxholes_mask_Q	Mask layer protecting areas of the Q-plane that should not be populated with flux-trapping holes — normally used to keep a proximity from important features.

Layer	Shorthand name	Description
28	fluxholes_MCM	Subtractive layer for the MCM-plane. This layer should only contain flux holes.
29	fluxholes_mask_MCM	Mask layer protecting areas of the MCM-plane that should not be populated with flux-trapping holes — normally used to keep a proximity from important features.
30*	JJ_consolidation	Consolidation layer using layers 31 and 32, whose overlap defines the Josephson Junctions through Manhattan shadow evaporation.
31	JJ_elec_vert	Vertical arms.
32	JJ_elec_hori	Horizontal arms.
35	JJ_undercut	Undercuts for angled depositions to alleviate lift-off.
40	JJ_patch	Areas used to create galvanic contact between GP and JJ layers by milling the metal oxide before deposition.
50	airbridge_feet	The layer which defines the base of the airbridge electrodes.
60	airbridge_etch	The protective area which defines the Al that remains after the etch.

* Layer 30 (JJ_consolidation) is a derived layer — the Josephson Junction is defined by the overlap of layers 31 and 32; layer 30 itself is not drawn directly.

Importing the Layer Convention

The matching .lyp file for this scheme is provided alongside this PDF — import it directly into KLayout rather than re-entering the table by hand:

1. Load it once — in KLayout: **File** → **Load Layer Properties**, and select the .lyp file.

2. (Optional) Load it automatically every time — go to **Tools** → **Manage Technologies**, enable “Load layer properties,” and point it at the file's path so it's available in the toolbar on every KLayout startup.

These steps are described here as they appear in the source wiki page; that page also includes screenshots of each dialog which aren't reproduced in this PDF — refer to the wiki directly if you have access, or ask the organizer if a step is unclear.